

**SYSTEM AND METHOD FOR INTEGRATED CIRCUIT DEVICE DESIGN AND  
MANUFACTURE USING OPTICAL RULE CHECKING TO SCREEN  
RESOLUTION ENHANCEMENT TECHNIQUES**

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**ABSTRACT OF THE DISCLOSURE**

A method of selecting a plurality of lithography process parameters for  
patterning a layout on a wafer includes simulating how the layout will print on the  
wafer for a plurality of resolution enhancement techniques (RETs), where each  
10 RET corresponds to a plurality of lithography process parameters. For each  
RET, the edges of structures within the simulated layout can be classified based  
on manufacturability. RETs that provide optimal manufacturability can be  
selected. In this manner, the simulation tool can be used to determine the  
optimal combination of scanner setup and reticle type for minimizing the variation  
15 in wafer critical dimension (CD).

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